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(54) Electrically erasable programmable read only memory.

(57) A single layer of polycrystalline silicon (poly-Si) is used in an EEPROM structure, which obviates the need to form a separate control gate and floating gate. The EEPROM utilizes three separate NMOS transistors: a write transistor (20), a read transistor (40), and a sense transistor (30). A thin tunnel oxide layer (55) separates the N+ source region (24) of the write transistor (20) from an N doped poly-Si layer (38) and capacitively couples the source region to the poly-Si layer. The poly-Si layer extends over the N+ source region (34) of the sense transistor (30) and is capacitively coupled to the source region (34) of the sense transistor (30) via a thin gate oxide insulating layer which is thicker than the oxide layer comprising the tunnel oxide layer. This poly-Si layer continues to extend over a channel region (35) separating the N+ source (34) and N+ drain regions (32) of the sense transistor (30), the poly-Si layer being separated from the channel via the thin gate oxide insulating layer. The drain (32) of the sense transistor (30) also acts as the source of the read transistor (40). The poly-Si layer (38) acts as the floating gate over the channel (35) of the sense transistor (30). Since the poly-Si floating gate (38) is both capacitively coupled to the source (34) of the sense transistor (30) and to the source (24) of the write transistor (20), no separate control gate or control gate electrode is needed (the source of the sense transistor acts as the control gate).

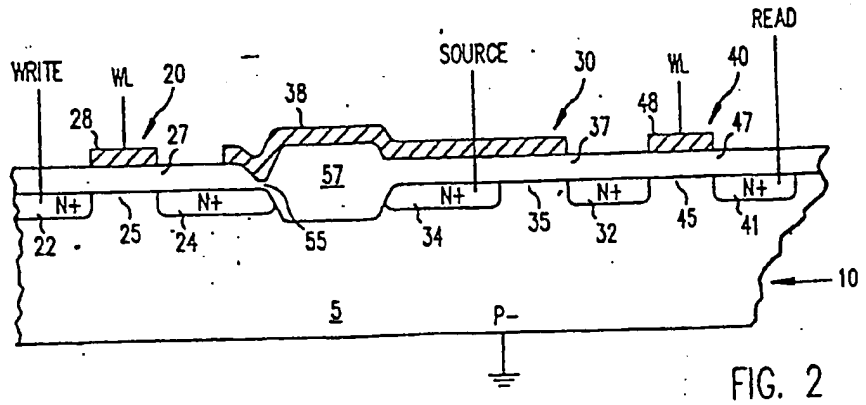

FIG. 2

EP 0 295 935 A1

Figure 6 is a graph showing the voltage threshold of the sense transistor in Figure 2 given various erase voltages and pulse widths, and

Figure 7 is a graph showing current through the sense transistor of Figure 2 given certain programming voltages and pulse widths.

Figure 2 shows an EEPROM memory cell 10 in accordance with the preferred embodiment of the invention. A P- type substrate 5 has five N+ type regions formed on and below its surface by standard diffusion techniques. These N+ type regions correspond to the source and drain regions of the three transistors which make up the EEPROM memory circuit. Write transistor 20 comprises drain 22, source 24, channel region 25, gate oxide layer 27 and control gate 28. Sense transistor 30 comprises drain 32, source 34, channel region 35, gate oxide layer 37, and N type polycrystalline silicon (poly-Si) floating gate 38. Read transistor 40 comprises drain 41, source 32, which is also the drain of sense transistor 30, channel region 45, gate oxide layer 47, and control gate 48. Poly-Si floating gate 38 is capacitively coupled to source 34 of sense transistor 30, via gate oxide layer 37 (approximately 300Å in thickness), and capacitively coupled to source 24 of write transistor 20 via tunnel oxide layer 55 (approximately 90Å in thickness). Poly-Si floating gate 38 also extends over channel region 35 of sense transistor 30 so that when a sufficient positive charge is on poly-Si floating gate 38, channel 35 will invert and conduct current between source 34 and drain 32 of sense transistor 30. Field oxide layer 57 insulates floating gate 38 from the underlying substrate 5 separating sense transistor 30 and write transistor 20.

Operation of the memory cell 10 will be described with reference to Figures 2 and 3. In Figure 3 word line WL is connected to control gates 28 and 48 of write transistor 20 and read transistor 40, respectively. Tunnel oxide layer 55 is represented by capacitor C_t while gate oxide layer 37 between source 34 of sense transistor 30 and poly-Si floating gate 38 is represented by capacitor C_g. Drain and source contacts are represented by D and S, respectively

The three operations of the memory circuit are write, erase, and read. The various voltages applied to the circuit of Figure 3 is shown in Table 3.

TABLE 3

	WL	Write	Read	Source	Substrate
Read	V_{cc}	ground	V_{sense}	ground	ground
Write	V_{pp}	V_{pp}	ground	ground	ground
Erase	V_{pp}	ground	V_{pp}	V_{pp}	ground

When N type poly-Si floating gate 38 is written upon, or programmed, floating gate 38 is given a positive charge by removing free electrons from floating gate 38. To accomplish this, first, a high programming voltage V_{pp} is applied to word line WL, which turns on write and read transistors 20 and 40. By turning on transistor 20, a write signal applied to drain 22 of write transistor 20 is coupled to source 24 of write transistor 20. Similarly, when transistor 40 is on, a read signal applied to drain 41 of read transistor 40 is coupled to source 32 of read transistor 40. Next, in order to program sense transistor 30, high programming voltage V_{pp} is applied to drain 22 of write transistor 20, and source 34 of sense transistor 30, as well as drain 41 of read transistor 40 and substrate 5, is grounded. Since source 24 of write transistor 20 is at a high voltage and source 34 of sense transistor 30 is grounded, voltage is capacitively coupled to poly-Si floating gate 38 due to the electric field created between source 24 and source 34 through gate oxide layer 37 and tunnel oxide layer 55.

Since the capacitance between source 24 and floating gate 38 across tunnel oxide layer 55 is very small (on the order of 0.004pF), and the capacitance between source 34 and floating gate 38 across gate oxide layer 37 is about ten times greater, a large percentage (on the order of 90%) of the voltage difference between source 24 and source 34 (i.e., V_{pp}) appears between source 24 and floating gate 38 across tunnel oxide layer 55. This voltage is sufficient to cause electron tunneling from floating gate 38 to source 24 of write transistor 20 through tunnel oxide layer 55, resulting in a net positive charge on floating gate 38. The positive charge is sufficient to turn on sense transistor 30 because floating gate 38 extends over channel region 35 of sense transistor 30. This indicates a logical 1 since current can flow through sense transistor 30 during a read operation.

To erase floating gate 38, high programming voltage V_{pp} is applied to word line WL as well as source 34 of sense transistor 30 and drain 41 of read transistor 40, while drain 22 of write transistor 20 and substrate 5 are grounded. In this biasing arrangement, the high voltage at source 34 of sense transistor 30

is capacitively coupled to floating gate 38 and almost all of high programming voltage V_{pp} appears across tunnel oxide layer 55 between floating gate 38 and grounded drain 24. This causes electrons from drain 24 to tunnel through tunnel oxide layer 55, resulting in a net negative charge on floating gate 38. Thus, channel 35 of sense transistor 30 is not inverted and sense transistor 30 is shut off.

When reading the state of sense transistor 30, operating voltage V_{cc}, which is less than programming voltage V_{pp}, is applied to word line WL, and voltage V_{sense} (usually $V_{cc}/2$) is applied to drain 41 of read transistor 40. Drain 22 of write transistor 20, as well as source 34 of sense transistor 30 and substrate 5, are grounded. A current flows between drain 41 and source 34 if sense transistor 30 is on, indicating a logical 1. If sense transistor 30 is off, current does not flow, indicating a logical 0.

Since sense transistor 30 and read transistor 40 are not subject to high voltage V_{pp} between their source and drain regions, their channel lengths may be made short to increase reading speed.

During the erase operation, source 34 and drain 32 of sense transistor 30 are at a high voltage while substrate 5 is grounded. This drives channel 35 into deep depletion, thus reducing the undesired parasitic capacitance between floating gate 38 and channel 35 and, hence, creating a higher coupling ratio during the erase operation, enabling faster erase times. During the writing operation, both source 34 and channel region 35 are grounded so no undesired parasitic capacitances exist.

Prior art cells which use a separate control gate above the floating gate, such as that shown in Figure 1, and apply the voltages shown in Table 2, incur a higher undesired capacitance between the floating gate and the substrate during erasing. This is because, during erasing of the floating gate, the source is floating or at a ground potential to prevent current from flowing through the transistor during erasing, and, consequently, the channel is not driven into deep depletion. To offset this higher capacitance between the floating gate and the substrate, a higher capacitance must be created between the control gate and the floating gate by increasing the area of the control gate. This undesirably increases the size of the EEPROM itself.

Prior art cells such as that shown in Figure 1 which apply the voltages shown in Table 1, incur a similar undesired capacitance between the floating gate and the substrate, as discussed above, but during the write operation.

Since the memory cell couples a greater voltage to floating gate 38, the tunnel oxide area under tunnel oxide layer 55 may be made smaller than the prior art tunnel oxide area, thus allowing less chance of defects in the formation of the thin tunnel oxide layer. In the preferred embodiment, the tunnel oxide area is approximately 1 micron^2. Prior art tunnel oxide areas are typically 10-15 microns^2. Thus, the invention enables an EEPROM to be formed which requires less chip area approximately 200 microns^2) than prior art devices, has faster read times, can be formed with less chance of defects, and can be made with less processing steps than prior art devices requiring a separate control gate.

In an alternative embodiment, shown in Figure 4, the EEPROM of Figure 2 uses a separate poly-Si control gate 36 to capacitively couple voltage to floating gate 38. Insulating, or coupling, layer 50 insulates control gate 36 and floating gate 38 from each other, and its thickness can be adjusted to obtain the desired capacitance between control gate 36 and floating gate 38. In this configuration, control gate 36 has applied to it the same voltages as the "Source" in Table 3. The added capacitive coupling from control gate 36 increases the coupling ratio during the write and erase operations. During erase, channel 35 is in deep depletion, further increasing the coupling ratio. In this alternative embodiment, coupling layer 50 is 300Å, with the remainder of the dimensions identical to the preferred embodiment described with reference to Figure 2.

In another embodiment, almost identical to that of Figure 4, in which two separate poly-Si layers are used, source 34 is not capacitively coupled to floating gate 38, and the voltage applied to it is irrelevant except during the read operations. However, the same reading, writing, an erasing voltages shown in Table 3 are applied to the remainder of the structure. The control gate has applied to it the same voltages as the "Source" in Table 3. To make negligible the capacitive coupling between source 34 and floating gate 38, a thick insulating layer such as field oxide layer 57, shown in Figure 4, extends over source 34 and separates source 34 from floating gate 38. In this embodiment, as in the embodiments shown in Figures 2 and 4, channel region 35 is in deep depletion during erasing, resulting in an increased coupling ratio and more efficient erasing of the charge on floating gate 38.

In another embodiment, shown in Figure 5, there is a separate N+ diffusion region 39, which acts as a control gate similar to control gate 36 in Figure 4, to capacitively couple voltage to floating gate 38. Insulating, or coupling, layer 37 insulates control gate 39 from floating gate 38. In this configuration, control gate 39 has applied to it the same voltages as the "Source" in Table 3. As in all embodiments, during, erase, channel 35 is in deep depletion, and, thus, there is negligible parasitic capacitance between channel 35 and floating gate 38.

Tests performed on an EEPROM in accordance with the preferred embodiment of Figure 2 showed that programming and erasing of the EEPROM can be satisfactorily accomplished using a programming and erasing voltage (V_{pp}) of 14 volts with a pulse width of about 300 µs. These results are shown in Figures 6 and 7. Figure 6 shows the resulting threshold voltage of sense transistor 30 when various V_{pp} voltages are applied to the EPPROM at various pulse widths. When the threshold voltage is a positive voltage, sense transistor 30 is off, indicating a logical 0 during the read operation. As sen from Figure 6, a V_{pp} of 14 volts for 300µs, while the EEPROM is biased in the erase mode, will raise the threshold voltage of sense transistor 30 to approximately 2 volts. Figure 7 shows the current through sense transistor 30, given a read voltage (V_{sense}) of 2 volts and a word line voltage (V_{cc}) of 5 volts. As seen, a V_{pp} of 14 volts for 300µs, while the EEPROM is biased in the programming, or write, mode, will enable a current of approximately 250µA to flow through sense transistor 30, indicating that sense transistor 30 is on and, thus, indicating a logical 1.

The preferred and alternative embodiments described are manufactured using well-known techniques, and their method of manufacture will be obvious to those skilled in the art.

This invention is by no means limited to the preferred and alternative embodiments described. While the invention has been particularly shown and described with reference to these preferred and alternative embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the scope of the invention as defined in the appended claims.

Claims

1. An EEPROM comprising a semiconductor substrate (5) of a first conductivity type having a top surface, first (34), second (32), and third (24) regions of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, a channel region (35) between said first and second regions, and a gate oxide layer (37) formed over said channel region (35),
characterized by

a tunnel oxide layer (55) formed over said third region (24); and

a floating gate (38) formed over said channel region (35), said floating gate (38) being capacitively coupled to said first region (34) via said gate oxide layer (37) and capacitively coupled to said third region (24) via said tunnel oxide layer (55), said tunnel oxide layer (55) being of a thickness to allow electron tunneling upon incurrence of a sufficient voltage potential between said floating gate (38) and said third region (24).

2. An EEPROM comprising:

a semiconductor substrate (5) of a first conductivity type having a top surface;

a first source region (24) of a write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a first drain region (22) of said write transistor (20) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a first channel region (25) of said write transistor (20) between said first source region (24) and said first drain region (22);

a first control gate (28) formed over and insulated from said first channel region (25);

a second source region (34) of a sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second drain region (32) of said sense transistor (30) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a second channel region (35) of said sense transistor (30) between said second source region (34) and said second drain region (32);

a gate oxide layer (37) formed over said second channel region (35) and said second source region (34) of said sense transistor (30);

a third source region (32) of a read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate, said third source region (32) also acting as said second drain region (32) of said sense transistor (30);

a third drain region (41) of said read transistor (40) of a conductivity type opposite that of said substrate formed on and below said surface of said substrate;

a third channel region (45) of said read transistor (40) between said third source region (32) and said third drain region (41) of said read transistor (40); and

a third control gate (48) formed over and insulated from said third channel region (45).

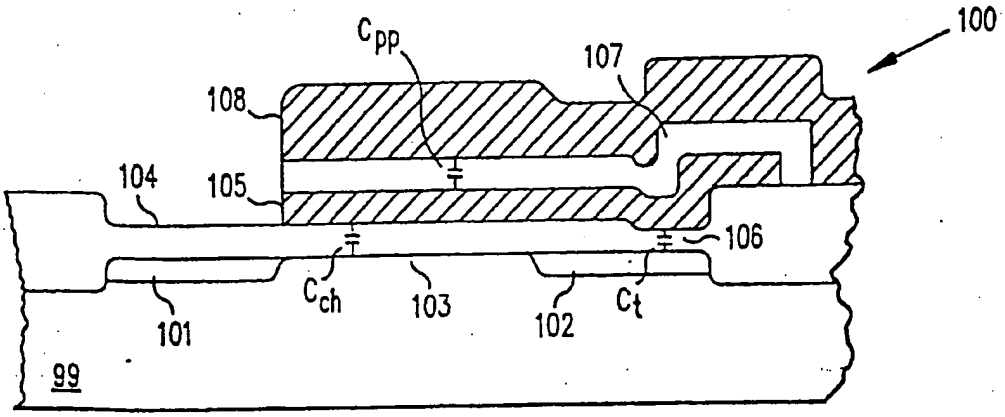

FIG. 1a
(Prior Art)

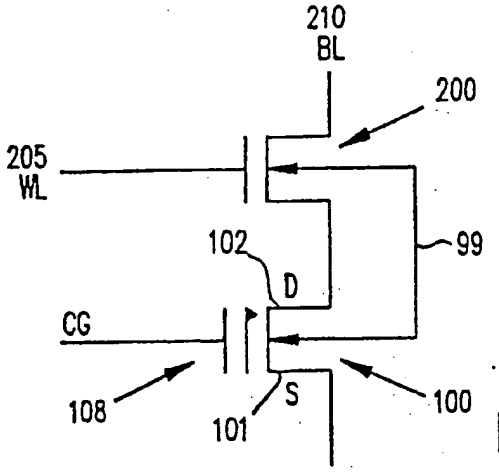

FIG. 1b
(Prior Art)

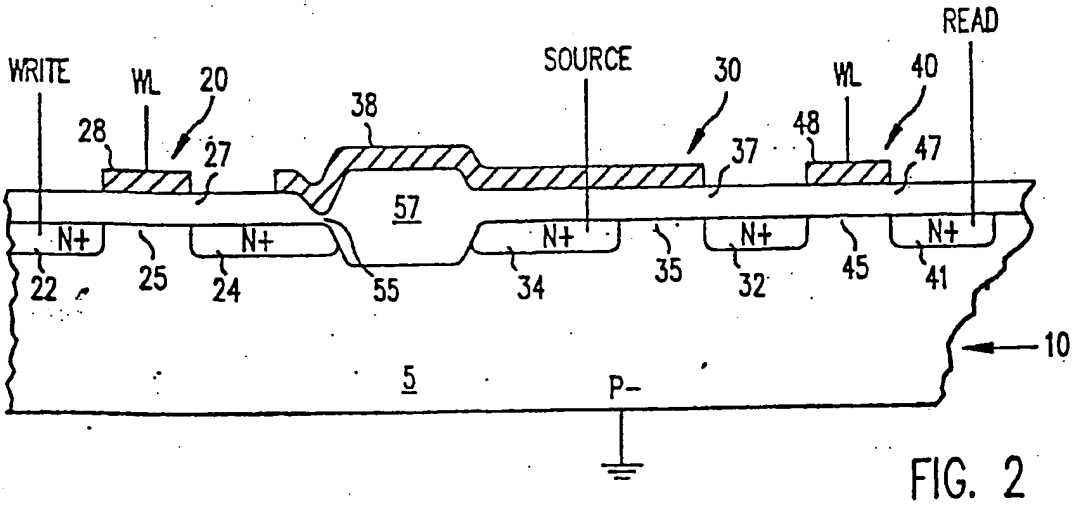

FIG. 2

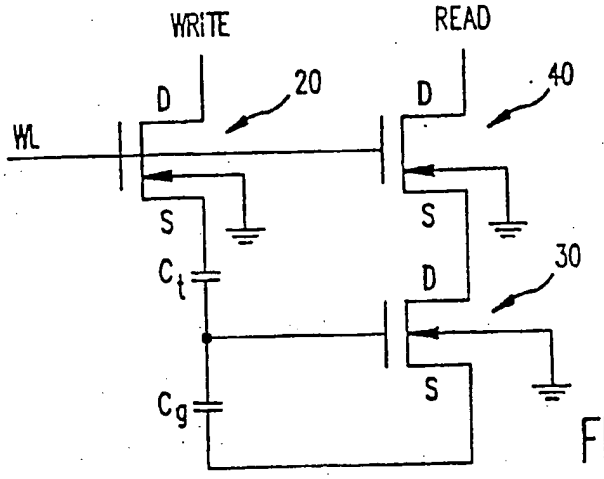

FIG. 3

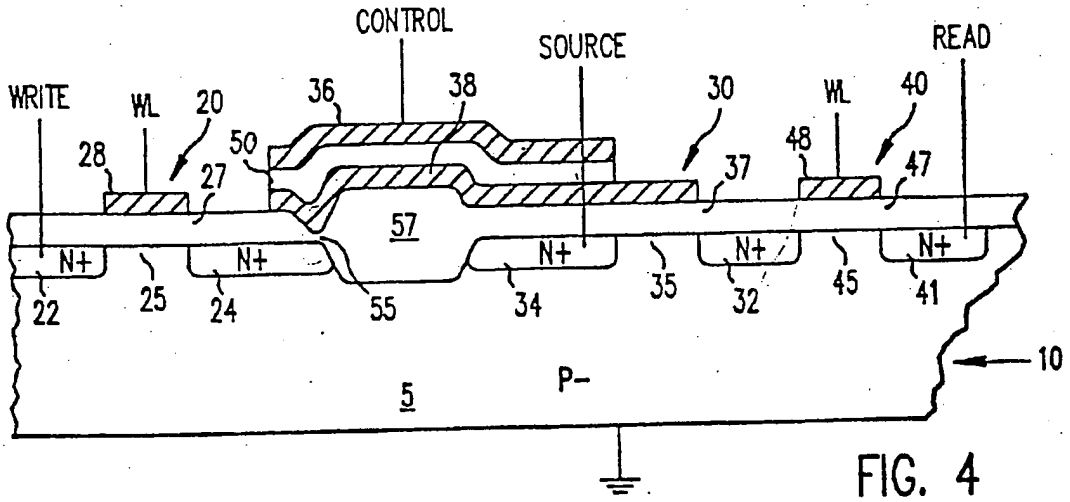

FIG. 4

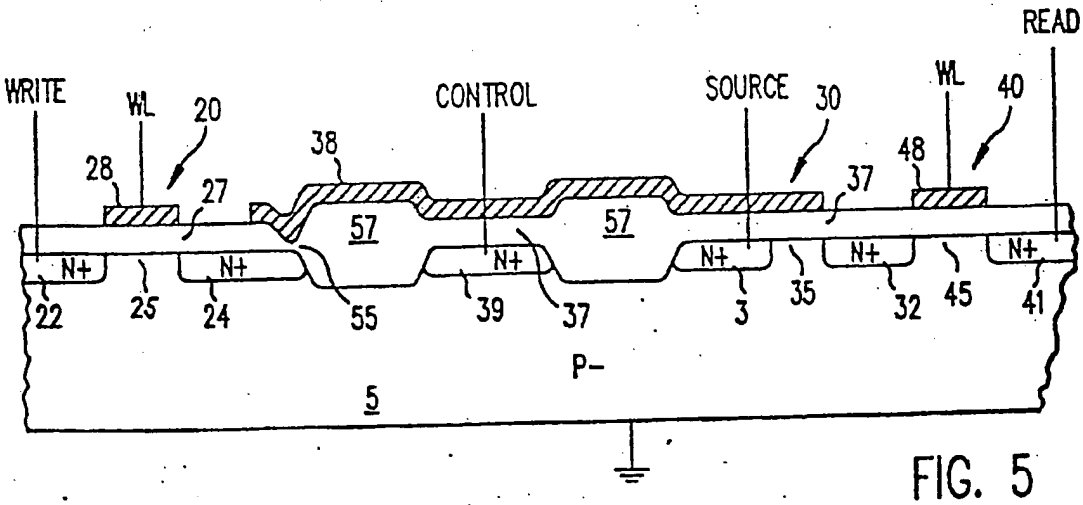

FIG. 5